REMARKS

In view of the above amendments and following remarks, reconsideration of the rejections contained in the Office Action of March 22, 2010 is respectfully requested.

Correction of Inventorship

The Examiner's attention is drawn to the filing of a Request for Correction of the Inventorship in the present application on January 22, 2010. The request asks to correct the inventorship by the addition of five named individuals as inventors in the application.

The Examiner is kindly requested to acknowledge receipt of the request and to proceed to amend the inventorship to add the five named individuals as inventors to the application.

Formal Matters

A number of minor editorial changes have been made to the specification to generally place the present application into better form. These have been presented in the form of a substitute specification. No new matter has been entered.

Rejections Presented in the Office Action

Claims 34-45 were under consideration by the Examiner. By the above amendments, claims 1-33, 36, 43 and 45-57 have been canceled without prejudice.

On page 2 of the Office Action, claims 34-39, 41 and 43 were rejected as being anticipated by Economikos et al., U.S. Patent 6,773,570 (Economikos). Further, on page 5 of the Office Action, claims 44 and 45 were rejected as being anticipated by Matsuda et al., U.S. Patent 6,375,823 (Matsuda). On page 6, claims 34-39, 41 and 43 were rejected as being unpatentable under 35 U.S.C. § 103(a) over Economikos in view of Chadda, U.S. Patent 7,025,860, or Emesh et al., U.S. Patent Publication 2002/0108861 (Emesh). On page 7, claims 40 and 42 were rejected as being unpatentable over Economikos in view of Chadda or Emesh and in further view of Matsuda.

However, it is respectfully submitted that the present invention clearly patentably defines over each of these references that have been cited by the Examiner, whether the references are considered individually or in combination. In particular, claims 34, 41 and 44, the independent

claims, have been amended to emphasize the distinctions present in the method of the present invention, and clearly patentably define over the references that have been cited.

The Claims as Amended Clearly Define Over the Cited Prior Art

The present invention is directed to a plating method in which the plating of a substrate having fine recesses for interconnects, covered with a seed layer, is carried out by supplying a plating solution and applying a plating voltage between the seed layer and an anode.

In accordance with the invention of amended independent claim 34, it is possible to suppress deposition of a plated film at raised portions of the seed layer while performing deposition of the plated film in the recesses of the seed layer. Note lines 1-11 of page 8 of the original specification, for example.

In particular, in claim 34, the plating solution is supplied between the surface of the seed layer and an anode that is spaced from the seed layer through a porous contact member. The substrate is plated by applying a plating voltage between the seed layer and the anode. The plating is performed while change of state of the plating voltage that is applied between the seed layer and the anode occurs, which change of state results from intermittence of the plating voltage. A change of pressing state between the porous contact member and the seed layer also occurs. The change of the state of the plating voltage is correlated, further, with the change of pressing state between the porous contact member and the seed layer. Thus in claim 34 the change of state of the plating voltage and the change of pressing state between the porous contact member and the seed layer occurs during the performance of the plating.

In the cited patent to Economikos, there is disclosed a process for plating and planarizing a workpiece such as a semiconductor wafer. The plating and the planarization of the plated layer are performed sequentially. During the plating process, a wafer carrier is adjusted so as to apply a downward force on the wafer so that the spacing between the wafer and a pad is less than the boundary layer thickness. Current is applied between the wafer and the anodes.

In Economikos, when the anode voltage is reversed so as to switch from plating to etching, the downward force on the wafer is varied in accordance with the anode voltage. That is, the downward force on the wafer is varied between plating and etching, but not during plating itself. The Examiner's detailed discussion of this on page 3 of the Office Action makes the sequential process clear, in fact, indicating that during the plating process, the wafer carrier is

adjusted to apply the downward force during plating, but that the change in voltage occurs when switching to etching.

By contrast, with the present invention the plating is performed while the change of state of the plating voltage and the change of pressing state between the porous contact member and the seed layer occur, with the change of state of the plating voltage being correlated with a change of pressing state. This is clearly not the case in Economikos, and for this reason claim 34 as amended clearly patentably defines over Economikos.

Independent claim 41 recites a plating method that includes (as now labeled) steps c and d comprising plating the substrate by applying current between the seed layer and the anode while filling a plating solution between the seed layer and the anode and pressing the porous member against the seed layer under a pressure, and, after plating the substrate, stopping the flowing current between the seed layer and the anode and then refreshing the plating solution between the seed layer and the anode after separating the porous member from the seed layer. Step e of claim 41 requires the repetition of steps c and d of the plating of the substrate and the refreshing of the plating solution.

Economikos provides no disclosure of plating the substrate, and then, after plating the substrate, stopping the flowing current, refreshing the plating solution between the seed layer and the anode after separation of the porous member from the seed layer, and then repeating these steps c and d.

As the Examiner notes on page 4 of the Office Action, in Economikos plating solution is continuously dispensed on pad 20 while the wafer rotates with respect to the pad. However, Economikos does not plate the substrate by flowing the current between the seed layer and the anode while filling a plating solution between the seed layer and the anode and pressing the porous member against the seed layer under pressure, after the plating, stopping the flowing of the current between the seed layer and the anode, and then refreshing the plating solution between the seed layer and the anode after separation of the porous member from the seed layer, as well as repeating these steps. Thus claim 41 clearly defines over Economikos.

Independent claim 44 now recites the plating method as including filling a plating solution between the seen layer and the anode while immersing the porous member and the plating solution, removing the plating solution that exists in a gap between the porous member and the seed layer by rotating the substrate and the porous member relative to each other while

pressing the porous member against the seed layer under pressure, and then plating the substrate by flowing current between the seed layer and the anode while pressing the porous member against the seed layer under pressure.

By removing the plating solution that exists in the gap between the porous member and the surface of the seed layer, after filling the plating solution between the seed layer and the anode while immersing the porous member and the plating solution, rotating the substrate and the porous member relative to each other under pressure, plating can then be performed in a state in which the entire surface of the porous member is uniformly brought into close contact with the surface of the substrate without increasing loads. Note for example the discussion at lines 16-23 of page 14 of the original specification.

Matsuda discloses a plating method for a substrate such as a semiconductor device. An impregnated member and a substrate are moved relative to each other in a direction of a contact plane. This is for preventing bubbles or dust in the plating solution that is supplied to the substrate surface from staying at one portion of the area between them. This helps to suppress defects in the plating film. A plating solution is supplied through the through holes 413 in anode 412 during scanning so the plating solution in the impregnated pad 411 will not run out. Note column 12, lines 26-32.

With the present invention, the plating solution that exists in the gap between the porous member and the seed layer is removed by rotation of the substrate and the porous member relative to each other while pressing them together under pressure. Then the substrate is plated by the flowing of the current between the seed layer and the anode under pressure. This is distinct from the method that is employed by Matsuda.

As such, it is respectfully submitted to be clear that claim 44 as amended is not anticipated by Matsuda. Indication of such is respectfully requested.

Independent claims 34 and 41, and dependent claims depending therefrom, were also rejected by the Examiner over Economikos in view of Chadda or Emesh. Chadda and Emesh were cited for the proposition of a porous polishing pad. However, these references do not otherwise cure the defects of Economikos with respect to meeting the limitations of independent claims 34 and 41, as well as their respective dependent claims.

Claims 40 and 42 were rejected as being unpatentable over Economikos in view of Chadda or Emesh and in further view of Matsuda. However, Matsuda does not cure the defects of Economikos with respect to meeting the limitations of independent claims 34 and 41, at least.

Accordingly, for all of the above reasons it is respectfully submitted that all of the claims that are now pending in the present application patentably define over all of the references that have been cited and applied by the Examiner. Indication of this is respectfully requested.

Conclusion

In view of the above it is respectfully submitted that the present application as a whole is in condition for allowance. All of the claims that are now pending in the application clearly patentably define over the prior art that has been cited by the Examiner. Indication of the allowability of the application as a whole is thus requested.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance, and the Examiner is requested to pass the case to issue. If the Examiner should have any comments or suggestions to help speed the prosecution of this application, the Examiner is requested to contact Applicants' undersigned representative.

Respectfully submitted,

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